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				Application Number	09/615,956-Conf. #003629
				Filing Date	July 13, 2000
				First Named Inventor	Kumi MIYACHI
				Art Unit	2133
				Examiner Name	E. T. Abraham
Sheet	1	of	1	Attorney Docket Number	1248-0509P

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS						
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	CA**	Satish, Keshava Iyengar, Tutorial on Design For Testability (DFT), "An ASIC Design Philosophy for testability from Chips to Systems," ASIC CONFERENCE AND EXHIBIT, PROCEEDINGS., SIXTH ANNUAL IEEE INTERNATIONAL, ROCHESTER, NY, USA, 27 September 1993, pages 130-139	

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